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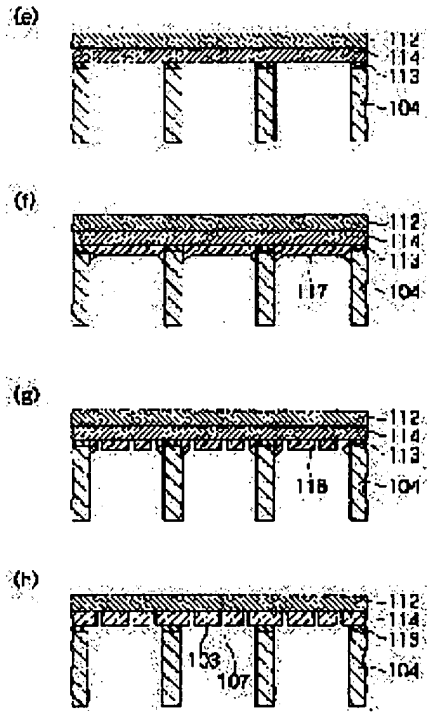
(54) MASK STAMPER, MASK AND ITS MANUFACTURING METHOD, AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a mask stamper that can increase efficiency in mask manufacture, and at the same time can improve the machining accuracy of a pattern, and to provide a mask, the method of manufacturing the mask, and the method of manufacturing a semiconductor device.

SOLUTION: This method of manufacturing the mask includes a process for forming a thin film 114 on one surface of a substrate, a process for forming a protection layer 112 on the thin film 114, a process for removing one portion of the substrate from the other side of the substrate for locally exposing the thin film 114, a process for providing a permeation section 107 where an electromagnetic wave with a specific wavelength permeates and a shielding section 103 where the electromagnetic wave is shielded at the exposed section of the thin film 114, and a process for removing a protection layer 112. The mask stamper and the mask are formed by the manufacturing method. The method of manufacturing the semiconductor device uses them.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the manufacturing method of the mask original recording for electron beam transcription mold lithography, a mask, and a mask, and the manufacturing method of a semiconductor device including an electron beam transcription mold lithography process especially about the manufacturing method of the mask original recording for lithography, a mask, and a mask, and the manufacturing method of a semiconductor device.
[0002]
[Description of the Prior Art]Utilization of electron beam transcription mold lithography (EPL;Electron beam Projection Lithography) is expected with the minuteness making of LSI, and high integration. As EPL to which utilization is advanced, PREVAIL (projection exposure with variable axis immersion lenses) (Journal H. C. Pfeiffer others.) which IBM and NIKON are developing jointly ofVacuum Science and Technology B17 p.2840 (1999) are mentioned.
[0003].SCALPEL (scattering with angular limitation in projection electron-beam lithography) which Lucent Technologies etc. are developing. (S. Proceedings of SPIE 3676 p.194(1999)) besides T. Stanton is mentioned. RIPURU, LEEPL (low.) which Tokyo Seimitsu and Sony are developing jointly energy electron-beam. proximity projection lithography (T. Utsumi and Journal of Vacuum Science and Technology B17 p.2897 (1999)) is mentioned.
[0004]PREVAIL and SCALPEL irradiate with the electron beam of about 100 keV, to transferring a mask pattern on a wafer, by LEEPL, irradiate with the electron beam of about 2 keV, and transfer a mask pattern on a wafer. LEEPL is a projection system of actual size to PREVAIL and SCALPEL(s) being usually 4 times as many reduction projection systems.
[0005]The stencil mask and the membrane mask are proposed as a mask used for EPL. A stencil mask is a mask which opened the hole (aperture) in the silicon thin film about 2

micrometers thick, and formed the pattern. On the other hand, a membrane mask is a mask which made heavy metals, such as chromium (Cr) and tungsten (W), deposit, and formed the pattern on the silicon nitride film about 150 nm thick.

[0006]When performing electron beam lithography using a stencil mask, an electron beam penetrates only an aperture part by no being scattered about, and image formation is carried out on resist. On the other hand, when performing electron beam lithography using a membrane mask, electron beams are scattered about in a heavy metal portion, and penetrate only portions other than a heavy metal. Resist is exposed by the electron beam which penetrated portions other than a heavy metal.

[0007]Both a stencil mask and the membrane mask of PREVAIL and SCALPEL are available respectively. A stencil mask is used, in order that the energy of an electron beam may be low in LEEPL and an electron beam may not penetrate a membrane mask to it.

[0008]A stencil mask and a membrane mask can also be formed using materials other than the above. To for example, both the membrane part for which the silicon nitride film was used conventionally, and the scatterer in which the heavy metal was used. the membrane mask using DLC (Diamond Like Carbon) is proposed (the 61st Japan Society of Applied Physics academic lecture -- collection [of meeting lecture drafts] (2000) No.2 p.619 7 a-X-5.) H. Journal of VacuumScience and Technology B18 (6) besides Yamashita p.3237 (2000). The stencil mask made from a diamond is also proposed for X-ray lithography (Journal of Vacuum Science and Technology B16 p.2772 (1998) besides H. Noguchi). Application to EPL of such a mask made from a diamond is also expected.

[0009]Hereafter, a conventional structure and manufacturing method of the mask for EPL are explained with reference to drawings. Drawing 10 (a) is a schematic diagram of the stencil mask used for PREVAIL.

Drawing 10 (b) is some (X-X') sectional views of drawing 10 (a).

As shown in drawing 10 (a), the stencil mask 201 has two or more membrane parts (membrane) 203 with a size of 1.13 mm x 1.13 mm in the silicon wafer 202 of 8 inch sizes. The membrane 203 is mutually separated by the beam called the strut 204. The width of the strut 204 is 170 micrometers. The strut 204 acts as a base material which maintains the mechanical strength of the stencil mask 201.

[0010]As shown in drawing 10 (b), as for the thickness of the membrane 203, it is 2 micrometers and the aperture 205 corresponding to the mask pattern of LSI is formed in the membrane 203. When forming the stencil mask 201 using an 8-inch wafer, the height of the strut 204 is set to 725 micrometers. The silicon oxide 207 is formed between the silicon layer 206 containing the membrane 203 and the strut 204. In the process of etching into the rear face of the silicon wafer 202, and forming the strut 204, the silicon oxide 207 is used as an etching stopper layer.

[0011]In order to manufacture the above stencil masks 201, as shown in drawing 11 (a), the SOI wafer 211 is produced first. The SOI wafer 211 has the silicon layer 206 via the silicon oxide 207 in one field of the silicon wafer 202, and has the rear-face side silicon oxide 212 in the field of another side of the silicon wafer 202. The SOI wafer 211 can be formed by for example, the SIMOX (separation by implantedoxygen) method or a lamination method.
[0012]Next, as shown in drawing 11 (b), the resist 213 is formed in the rear-face side of the SOI wafer 211 by the pattern (refer to drawing 10) of the strut 204. After applying the resist 213 to the whole surface with a spin coat, it forms by performing exposure and development. Dry etching is performed to the rear-face side silicon oxide 212 and the silicon wafer 202 by using resist 213 as a mask from the rear-face side of the SOI wafer 211. Thereby, the strut 204 which consists of silicon is formed.
[0013]Next, as shown in drawing 11 (c), it etches into the silicon oxide 207 by the side of the surface by using the strut 204 as a mask. Then, the resist 213 is removed. Next, as shown in drawing 11 (d), the resist 214 of a predetermined pattern is formed on the silicon layer 206. After applying the resist 214 to the whole surface, for example with a spin coat, it forms by performing exposure and development.
[0014]Next, dry etching is performed to the silicon layer 206 by using resist 214 as a mask. Thereby, as shown in drawing 10 (b), the membrane 203 which has the aperture 205 of a predetermined pattern is formed. Then, the rear-face side silicon oxide 212 and the resist 214 are removed. The stencil mask 201 is formed of the above process.
[0015]Drawing 12 (a) is a schematic diagram of the membrane mask used for SCALPEL. Drawing 12 (b) is some (X-X') sectional views of drawing 12 (a).
As shown in drawing 12 (a), the membrane mask 221 has two or more membrane parts (membrane) 222 with a size of 1 mm x 12 mm in the silicon wafer 202 of 8 inch sizes. The membrane 222 is mutually separated by the beam called the strut 204. The width of the strut 204 is 300 micrometers. The strut 204 acts as a base material which maintains the mechanical strength of the membrane mask 221.
[0016]As shown in drawing 12 (b), the membranes 222 are some supporters who consist of the silicon nitride film 223, and the thickness of the silicon nitride film 223 is 150 nm. On the silicon nitride film 223, the scatterer 224 corresponding to the mask pattern of LSI is formed. As the scatterer 224, chromium and a heavy metal like tungsten are used, for example, and the thickness of the scatterer 224 is about 30-50 nm. When forming the membrane mask 221 using an 8-inch wafer, the height of the strut 204 is set to 725 micrometers.
[0017]In order to manufacture the above membrane masks 221, as shown in drawing 13 (a), the silicon nitride film 223 is first formed on the silicon wafer 202. A chromium layer and a tungsten layer are formed in the upper layer in order, and the cascade screen 225 is formed. The thickness of a chromium layer shall be 5 nm and the thickness of the tungsten layer of the

upper layer shall be 25 nm. Although not illustrated, rear-face side silicon oxide may be provided in the silicon wafer 202 like drawing 11 (a).

[0018]Next, as shown in drawing 13 (b), the resist 226 is formed in the rear-face side of the silicon wafer 202 by the pattern (refer to drawing 12) of the strut 204. After applying the resist 226 to the whole surface with a spin coat, it forms by performing exposure and development. Dry etching is performed by using resist 226 as a mask from the rear-face side of the silicon wafer 202. Thereby, the strut 204 which consists of silicon is formed. Then, the resist 226 is removed.

[0019]Next, as shown in drawing 13 (c), the resist 227 is applied with a spin coat the whole surface on the cascade screen 225. Next, as shown in drawing 13 (d), exposure and development are performed to the resist 227, and the resist 228 corresponding to the mask pattern of LSI is formed. Next, dry etching is performed to the cascade screen 225 by using resist 228 as a mask. Thereby, as shown in drawing 12 (b), the scatterer 224 of a predetermined pattern is formed. Then, the resist 228 is removed. The membrane mask 221 is formed of the above process.

[0020]Drawing 14 (a) is a schematic diagram of the stencil mask used for LEEPL. Drawing 14 (b) is some sectional views of drawing 14 (a).

As shown in drawing 14 (a), the stencil mask 231 has the membrane part (membrane) 203 with a size of 20 mm x 20 mm in the silicon wafer 202 of 8 inch sizes. The silicon wafer 202 around the membrane 203 is called the strut 204, and acts as a base material which maintains the mechanical strength of the stencil mask 231.

[0021]As shown in drawing 14 (b), as for the thickness of the membrane 203, it is 500 nm and the aperture 205 corresponding to the mask pattern of LSI is formed in the membrane 203. When forming the stencil mask 231 using an 8-inch wafer, the height of the strut 204 is set to 725 micrometers. The silicon oxide 207 is formed between the silicon layer 206 containing the membrane 203 and the strut 204. In the process of etching into the rear face of the silicon wafer 202, and forming the strut 204, the silicon oxide 207 is used as an etching stopper layer.

[0022]In order to manufacture the above stencil masks 231, as shown in drawing 15 (a), the SOI wafer 211 which has the silicon layer 206 via the silicon oxide 207 in one field of the silicon wafer 202 is produced first. Next, as shown in drawing 15 (b), the resist 232 is formed in the rear-face side of the SOI wafer 211 by the pattern (refer to drawing 14) of the strut 204. After applying the resist 232 to the whole surface with a spin coat, it forms by performing exposure and development. It etches into the silicon wafer 202 by using resist 232 as a mask from the rear-face side of the SOI wafer 211. Then, the resist 232 is removed.

[0023]The strut 204 is not formed with high density like [the stencil mask 231 for LEEPL is an actual size mask, and its area of the membrane 203 is large, and] the stencil mask 201 for PREVAIL shown in drawing 10. Therefore, the section of the strut 204 may serve as tapered

shape, and can form the strut 204 by wet etching.

[0024]Next, as shown in drawing 15 (c), the resist 233 is applied with a spin coat the whole surface on the silicon layer 206. Then, as shown in drawing 15 (d), exposure and development are performed to the resist 233, and the resist 234 corresponding to the mask pattern of LSI is formed. Dry etching is performed to the silicon layer 206 by using resist 234 as a mask. Thereby, the aperture 205 of a predetermined pattern is formed. Then, the resist 234 is removed as shown in drawing 14 (b). The stencil mask 231 is formed of the above process.

[0025]

[Problem(s) to be Solved by the Invention]However, according to the manufacturing method of a semiconductor device including the mask manufacture process according to the manufacturing method of the above-mentioned conventional mask, or it, etching for forming the strut 204 in the rear-face side of a wafer takes a long time. In order to require several hours for etching a part for the thickness of the silicon wafer 202 by dry etching especially, the turn around time (TAT) from the end of a design pattern to mask completion becomes long.

[0026]If it etches into a wafer back face and a strut is beforehand formed before the end of a design pattern, as shown in drawing 11 (c), drawing 13 (b), or drawing 15 (b), after between the struts 204 has become the membrane parts 203 and 222, mask original recording must be kept or carried. Thus, where the membrane parts 203 and 222 are formed, since the mechanical strength of mask original recording is falling remarkably, it is easy to damage mask original recording during storage or conveyance, and becomes a factor which reduces the yield of a mask. In order to avoid this, formation of the strut 204 is started after the end of a design pattern in many cases, and shortening of TAT is made difficult as a result.

[0027]According to the manufacturing method of the above-mentioned conventional mask, after forming the strut 204 in the rear-face side of the silicon wafer 202, the resist of the mask pattern of LSI is formed in the surface side of the silicon wafer 202 (refer to drawing 11 (d), drawing 13 (d), or drawing 15 (d)). Therefore, when forming resist in the surface side of the silicon wafer 202, it is necessary to perform alignment from the both-sides side of the silicon wafer 202. It is difficult to perform alignment from such both sides with high precision, and the yield of a mask falls easily. A double-sided aligner is also required.

[0028]According to the manufacturing method of the above-mentioned conventional mask, after applying resist to the surface side of the silicon wafer 202, the baking powder of resist becomes uneven easily. Baking powder lays the silicon wafer 202 on a hot plate, and is performed. Since the silicon wafer 202 is supported by the strut 204 at this time, heat conduction from a hot plate becomes uneven in a wafer surface. When baking powder becomes uneven, the process tolerance of a pattern falls.

[0029]When dry etching is performed to the silicon layers 206 and 232 of the stencil masks 201 and 231 and the aperture 205 is formed, Or also when performing dry etching to the

cascade screen 225 of the membrane mask 221 and forming the scatterer 224, the silicon wafer 202 is supported by the strut 204. Therefore, a crevice is formed between the membrane parts 203 and 222 and the stage of an etching device.
[0030]Thus, in the state where the mechanical strength of the whole mask fell, if the influence of generation of heat at the time of etching, etc. is added, in being the worst, it will damage a mask. Even if it is a case where a mask is not damaged, if a mask changes by generation of heat at the time of etching, etc., the membrane parts 203 and 222 will no longer be supported stably. Thereby, the process tolerance of a pattern falls or a pattern dimension shows dispersion.
[0031]This invention is made in view of the above-mentioned problem, and is a thing.
The purpose is to provide the manufacturing method of the mask original recording which this invention raises the efficiency of mask manufacture, and can improve the process tolerance of a pattern, a mask, and a mask, and the manufacturing method of a semiconductor device.

[0032]
[Means for Solving the Problem]This invention is characterized by mask original recording comprising the following, in order to attain the above-mentioned purpose.
A thin film which makes electromagnetic waves of predetermined wavelength irradiated at the 1st page side penetrate to the 2nd page side locally.
A protective layer removable from said thin film formed on said 1st page of said thin film.
A thin film supporting part which was formed in a part on said 2nd page of said thin film so that said electromagnetic wave which penetrated said thin film might not be intercepted and which supports said thin film.

[0033]Suitably, said thin film has an aperture which said electromagnetic wave penetrates, and mask original recording of this invention intercepts said electromagnetic wave in portions other than said aperture. Mask original recording of this invention is suitably characterized by said electromagnetic wave being an electron beam, X-rays, EUV light, or an ion beam.
[0034]Mask original recording of this invention has further suitably the 1st etching stopper layer that can make an etch rate later than said thin film supporting part between layers of said 2nd page and said thin film supporting part of said thin film. Mask original recording of this invention has further suitably the 2nd etching stopper layer that can make an etch rate later than said protective layer between layers of said protective layer and said 1st page of said thin film.
[0035]Suitably, said thin film has further the scatterer which scatters about for it and intercepts said electromagnetic wave on said 2nd page of a portion in which said thin film supporting part is not formed, and mask original recording of this invention penetrates said electromagnetic

wave in portions other than said scatterer. Mask original recording of this invention is suitably characterized by said electromagnetic wave being an electron beam, X-rays, EUV light, or an ion beam.

[0036]Mask original recording of this invention has further suitably the 1st etching stopper layer that can make an etch rate later than said thin film supporting part between layers of said 2nd page and said thin film supporting part of said thin film. Mask original recording of this invention has further suitably the 2nd etching stopper layer that can make an etch rate later than said protective layer between layers of said protective layer and said 1st page of said thin film.

[0037]Mask original recording of this invention is suitably formed in shape to which said thin film supporting part has at least one rectangular opening on said 2nd page of said thin film. As for mask original recording of this invention, said thin film supporting part is formed on said 2nd page of said thin film still more suitably in shape in which two or more rectangular openings were arranged by matrix form.

[0038]Also when according to mask original recording of this invention a mechanical strength becomes high and mask original recording is kept or carried before mask use by having a protective layer, breakage of mask original recording is prevented. According to mask original recording of this invention, it is possible to advance manufacture of a mask, after a mask has been protected by protective layer. Therefore, breakage of mask original recording in a manufacturing process is prevented, and a yield of a mask improves.

[0039]This invention is characterized by mask original recording comprising the following, in order to attain the above-mentioned purpose.

Thin film.

A protective layer removable from said thin film formed on said 1st page of said thin film.

A thin film supporting part which was formed in a part on said 2nd page of said thin film and which supports said thin film.

Mask original recording of this invention has further suitably the 1st etching stopper layer that can make an etch rate later than said thin film supporting part between layers of said 2nd page and said thin film supporting part of said thin film. Mask original recording of this invention has further suitably the 2nd etching stopper layer that can make an etch rate later than said protective layer between layers of said protective layer and said 1st page of said thin film.

[0040]Or mask original recording of this invention has further suitably a filter layer which consists of material which are scattered about and intercepts electromagnetic waves of predetermined wavelength formed in a portion in which said thin film supporting part on said 2nd page of said thin film is not formed. Mask original recording of this invention has further suitably the 1st etching stopper layer that can make an etch rate later than said thin film supporting part between layers of said 2nd page and said thin film supporting part of said thin

film.

[0041]Mask original recording of this invention has further suitably the 2nd etching stopper layer that can make an etch rate later than said protective layer between layers of said protective layer and said 1st page of said thin film. Mask original recording of this invention is suitably formed in shape to which said thin film supporting part has at least one rectangular opening on said 2nd page of said thin film. As for mask original recording of this invention, said thin film supporting part is formed on said 2nd page of said thin film still more suitably in shape in which two or more rectangular openings were arranged by matrix form.

[0042]This raises a mechanical strength of mask original recording in the state where a thin film supporting part and a thin film were formed, and it becomes possible to secure as stock. Therefore, TAT of mask manufacture is shortened. As for mask original recording with which a mechanical strength was reinforced by protective layer, it is possible to also make it circulate.

[0043]This invention is characterized by a mask comprising the following, in order to attain the above-mentioned purpose.

A thin film which makes electromagnetic waves of predetermined wavelength irradiated at the 1st page side penetrate to the 2nd page side locally.

A thin film supporting part which was formed in a part on said 2nd page of said thin film so that said electromagnetic wave which penetrated said thin film might not be intercepted and which supports said thin film.

Scatterer which was formed in a portion in which said thin film supporting part on said 2nd page of said thin film is not formed and which are scattered about and intercepts said electromagnetic wave.

[0044]It becomes easy for this to provide a protective layer removable easily before use of a mask in the 1st page side of a thin film of a mask. Therefore, a mask is prevented from being damaged in a manufacturing process of a mask, and it becomes possible to raise a yield of a mask.

[0045]In order to attain the above-mentioned purpose, a manufacturing method of a mask of this invention, A process of forming a thin film in one field of a substrate, and a process of forming a protective layer on said thin film, Said some of substrates are removed from the field side of another side of said substrate, and it has a process of providing a process at which said thin film is exposed locally, a transparent part which electromagnetic waves of predetermined wavelength penetrate to an exposed portion of said thin film, and a blocking section by which said electromagnetic wave is intercepted, and the process of removing said protective layer.

[0046]A process in which a manufacturing method of a mask of this invention provides said transparent part and said blocking section suitably, A part of exposed portion of said thin film is removed from said substrate side, an aperture is formed, and a process of making portions

other than said aperture into said blocking section is included by making said aperture into said transparent part.

[0047]This invention is characterized by a manufacturing method of a mask comprising the following.

A process which a process of providing said transparent part and said blocking section sprays resist on an exposed portion of said thin film at least still more suitably, and is applied.

A process of performing exposure and development to said resist, and transferring a predetermined mask pattern.

A process of etching into said thin film by using said resist as a mask, and forming said aperture.

A process of removing said resist.

[0048]As for a manufacturing method of a mask of this invention, still more suitably, making said resist spray from a nozzle, a process of spraying said resist moves at least one side of said nozzle and said substrate, and includes a process of performing a scan by said nozzle in said exposed portion.

[0049]Or a manufacturing method of a mask of this invention suitably, A process of forming a filter layer where a process of providing said transparent part and said blocking section becomes an exposed portion of said thin film from material which are scattered about and intercepts said electromagnetic wave, A process of making a limited residual of said filter layer into said blocking section is included by making into a transparent part a portion which removed said a part of filter layer and from which said filter layer was removed.

[0050]This invention is characterized by a manufacturing method of a mask comprising the following.

A process which a process of providing said transparent part and said blocking section sprays resist on the surface of said filter layer suitably, and is applied.

A process of performing exposure and development to said resist, and transferring a predetermined mask pattern.

A process of etching into said filter layer by using said resist as a mask.

A process of removing said resist.

As for a manufacturing method of a mask of this invention, still more suitably, making said resist spray from a nozzle, a process of spraying said resist moves at least one side of said nozzle and said substrate, and includes a process of performing a scan by said nozzle in said exposed portion.

[0051]Suitably, before a manufacturing method of a mask of this invention forms said thin film in one field of said substrate, A process of having further the process of forming the 1st etching stopper layer that can make an etch rate late in said one field, and forming said thin film in it

rather than said substrate includes a process of forming said thin film via said 1st etching stopper layer on said substrate.

[0052]Suitably, before a manufacturing method of a mask of this invention forms a protective layer on said thin film, A process of having further the process of forming the 2nd etching stopper layer that can make an etch rate late, and forming said protective layer rather than said protective layer on said thin film includes a process of forming said protective layer via said 2nd etching stopper layer on said thin film.

[0053]A process from which a manufacturing method of a mask of this invention removes said some of substrates suitably includes dry etching or wet etching of said substrate. A process from which a manufacturing method of a mask of this invention removes said some of substrates suitably includes a process at which said thin film is exposed with at least one rectangular shape. As for a manufacturing method of a mask of this invention, a process of removing said some of substrates includes still more suitably a process at which said thin film is exposed with two or more rectangular shape arranged by matrix form.

[0054]Thereby, it becomes unnecessary to align a photolithography process by both sides of a wafer, and alignment becomes easy. Therefore, a yield of a mask can be raised. According to the manufacturing method of a mask of this invention, when etching into a thin film or a filter layer, a substrate is stably supported by the whole protective layer surface. Therefore, breakage of a thin film at the time of etching is prevented. Since a substrate is stably supported by the whole protective layer surface also when performing baking powder of resist, the baking powder of the resist is carried out uniformly, and size dispersion of a resist pattern can be made small.

[0055]In order to attain the above-mentioned purpose, a manufacturing method of a semiconductor device of this invention, A process of forming a mask for lithography which has a predetermined mask pattern, It is a manufacturing method of a semiconductor device which has the process of irradiating with electromagnetic waves via said mask for lithography on a substrate, and transferring said mask pattern to said substrate, A process of forming said mask for lithography, A process of forming a thin film in one field of a mask base material, and a process of forming a protective layer on said thin film, A process which removes said some of mask base materials from the field side of another side of said mask base material and at which said thin film is exposed locally, It has a process of providing a transparent part which electromagnetic waves of predetermined wavelength penetrate to an exposed portion of said thin film, and a blocking section by which said electromagnetic wave is intercepted, and the process of removing said protective layer.

[0056]Since TAT of a mask manufacture process is shortened and a yield of a mask improves by this, a manufacturing cost of a semiconductor device can be reduced. Since a mask pattern is formed with high precision, transfer performance of a mask pattern can improve and a yield

of a semiconductor device can be raised.

[0057]

[Embodiment of the Invention]Below, the embodiment of the manufacturing method of the mask original recording of this invention, a mask, and a mask and the manufacturing method of a semiconductor device is described with reference to drawings.

(Embodiment 1) Drawing 1 (a) is a schematic diagram of the stencil mask for electron beam transcription mold lithography manufactured by the mask manufacturing method of this embodiment, and drawing 1 (b) is the perspective view which expanded a part of drawing 1 (a) (A). Drawing 2 (a) is a sectional view in X-X' of drawing 1 (a). The stencil mask 101 shown in drawing 1 and drawing 2 is applicable to PREVAIL, for example.

[0058]The stencil mask 101 has two or more membrane parts (membrane) 103 with a size of 1.13 mm x 1.13 mm, for example in the silicon wafer 102 of 8 inch sizes. The thickness of the membrane 103 is about 2 micrometers. The membrane 103 is mutually separated by the beam called the strut 104. The width of the strut 104 is 170 micrometers.

[0059]The strut 104 acts as a base material which maintains the mechanical strength of the stencil mask 101. If it is a range in which the membrane 103 is held although the thickness of the strut 104 is set to 725 micrometers when forming the stencil mask 101 using an 8-inch wafer, the thickness of the strut 104 can be changed.

[0060]The membrane 103 is provided with the following as shown in drawing 1 (b).

The pattern space 105 of 1 mm square with which an electron beam is irradiated.

The margin called the skirt board 106 of the circumference.

The aperture 107 shown in drawing 2 (a) is formed in the pattern space 105 shown in drawing 1 (b).

[0061]First, in order to manufacture the above stencil masks 101, as shown in drawing 2 (b), the SOI wafer 111 is produced and the protective layer 112 is formed in the surface side of the SOI wafer 111. The SOI wafer 111 has the silicon layer 114 via the silicon oxide 113 in one field of the silicon wafer 102, and has the rear-face side silicon oxide 115 in the field of another side of the silicon wafer 102.

[0062]In the process of etching into the rear face of the silicon wafer 102, and forming the strut 104, the silicon oxide 113 is used as an etching stopper layer. Hereafter, in order to distinguish from other etching stopper layers, let for convenience the etching stopper layer provided for such the purpose be the 1st etching stopper layer.

[0063]The SOI wafer 111 can be formed by for example, the SIMOX method or a lamination method. The thickness of the silicon wafer 102 is 725 micrometers, the thickness of the silicon oxide 113 is 50 nm, and the thickness of the silicon layer 114 is 2 micrometers.

[0064]Although not illustrated, the 2nd etching stopper layer that consists of rutheniums etc., for example may be formed between the layers of the silicon layer 114 and the protective layer

112. Thereby, when removing the protective layer 112 from the silicon layer 114, the terminal point of etching can be clarified. However, the case where etching quantity is controllable by control of the etching condition which includes etching time, for example with high precision, When monitoring reaction production gas in dry etching and checking etching quantity by in situ, it is not necessary to necessarily provide the 2nd etching stopper layer.

[0065]When dry etching for wafer thickness is performed by using resist as a mask, resist is also etched and it may stop being able to form a pattern, although it is not necessary to necessarily form the rear-face side silicon oxide 115. As an offset film for preventing this, about 100-nm silicon oxide may be formed in the rear face of the silicon wafer 102, for example. The rear-face side silicon oxide 115 can be formed with chemical vapor deposition (CVD;chemical vapor deposition). In not forming the rear-face side silicon oxide 115 in particular by CVD etc., a natural oxidation film about several nanometers thick turns into the rear-face side silicon oxide 115.

[0066]As the protective layer 112, a 500-nm-thick polysilicon layer is formed by CVD, for example. The material of the protective layer 112 should just be a material easily removable by etchant or the etching condition into which the silicon layer 114 is not etched. Thereby, after forming the aperture 107 in the membrane 103, the protective layer 112 can be removed, without doing damage to the membrane 103, as shown in drawing 2 (a). The layer which consists of materials, such as SiN, SiO_2, aluminum, or Cr, instead of a polysilicon layer may be formed as the protective layer 112. The thickness of the protective layer 112 should just be the thickness which can fully reinforce the intensity of the silicon layer 114 used as the membrane 103.

[0067]Next, the resist 116 is formed in the rear-face side of the silicon wafer 102 as shown in drawing 2 (c). The resist 116 is formed with the pattern of the strut 104 shown in drawing 1, i.e., the pattern which opened the interval whose square of 1.13 mm x 1.13 mm is 170 micrometers, and was located in a line with matrix form. After applying the resist 116 to the whole surface with a spin coat, it forms by performing exposure and development.

[0068]Then, dry etching is performed to the silicon wafer 102 by using resist 116 as a mask from the rear-face side of the SOI wafer 111. Fluorine system gas, such as for example, SF_6 and NF_3, is used for this dry etching as etching gas. Thereby, the strut 104 which consists of silicon is formed.

[0069]Next, as shown in drawing 2 (d), it etches into the silicon oxide 113 by using the strut 104 as a mask. Let this etching be the wet etching which used fluoric acid. Thereby, the silicon oxide 113 of membrane 103 portion shown in drawing 1 is removed. Then, the resist 116 is removed as shown in drawing 3 (e). The rear-face side silicon oxide 115 is also removed if needed.

[0070]Since the mechanical strength of a mask fell by forming a strut according to the manufacturing method of the conventional mask, it was difficult to keep or carry mask original recording, where a strut is formed. According to the manufacturing method of the mask of this embodiment, the mechanical strength of mask original recording is maintained also after formation of the strut 104 by forming the protective layer 112 to it.
[0071]Therefore, also when dry etching is beforehand performed to the silicon wafer 102 and the strut 104 is formed before the design pattern was completed, the breakage under storage of mask original recording is prevented. If the dry etching for forming the strut 104 forms the strut 104 beforehand and secures it as stock in order that it may require a long time, shortening of TAT from a design pattern to mask completion of it will be attained. Since the breakage at the time of carrying mask original recording where the strut 104 is formed is also reduced, it is also possible to supply as a product the mask original recording of the stage shown in drawing 3 (e) if needed.
[0072]Next, the resist 117 is applied to the field by the side of the strut 104 of the silicon layer 114 as shown in drawing 3 (f). As the resist 117, positive-resist FEP102 (made by Fuji Photo Film Olin) is applied, for example. Since unevenness by the strut 104 exists in a resist application side, resist cannot be applied by methods, such as a spin coat. The method of applying resist to such a rugged surface, For example, the patent No. 3084339 gazette, JP,10-321493,A, JP,8-306614,A, JP,11-329938,A, or the collection of the 61st Japan Society of Applied Physics academic lecture meeting lecture drafts (2000) No.2 p.593 It is indicated to 4 a-X-1.
[0073]According to the method given in the patent No. 3084339 gazette, carry resist application liquid on a substrate, and coating liquid is thinly extended on a scanner plate to a substrate, and a coat is uniformly pressed on a substrate with the air pressure which blows off from the slit shaped nozzle which follows immediately after a scanner plate.
[0074]A resist film formation method given in JP,10-321493,A is provided with the following.
The process of applying resist to a substrate face.
For example, the process of heating the mask of a substrate, and cooling the upper surface, deteriorating some resist application films, and forming a deterioration layer and a non-deteriorating layer.
The process of removing a non-deteriorating layer.

[0075]According to the resist application method given in JP,8-306614,A, resist is applied to an entire substrate by moving a substrate or a nozzle and spraying resist on mist shape from a nozzle. According to the coating method given in JP,11-329938,A, processing agents, such as resist application liquid, are supplied from a nozzle, providing a nozzle in two or more positions which separated the prescribed interval, and moving those nozzles and processed boards

relatively.

[0076]Collection of the 61st Japan Society of Applied Physics academic lecture meeting lecture drafts (2000) No.2 p.593 In 4 a-X-1. In the nozzle scan applying method make the super-thin nozzle which trickles resist move reciprocately to a y direction, and make a x direction carry out constant-speed movement of the substrate simultaneously, the result of having applied resist under thinner atmosphere is indicated. In the usual spreading, if resist is applied under thinner atmosphere to thickness increasing by an edge part, local increase of thickness will be controlled.

* NOTICES *

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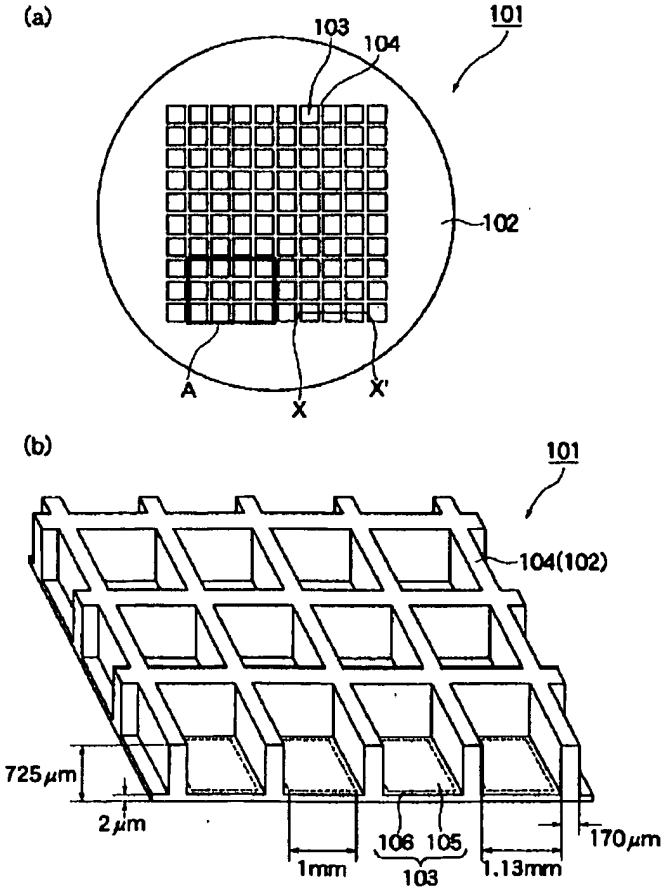
damages caused by the use of this translation.

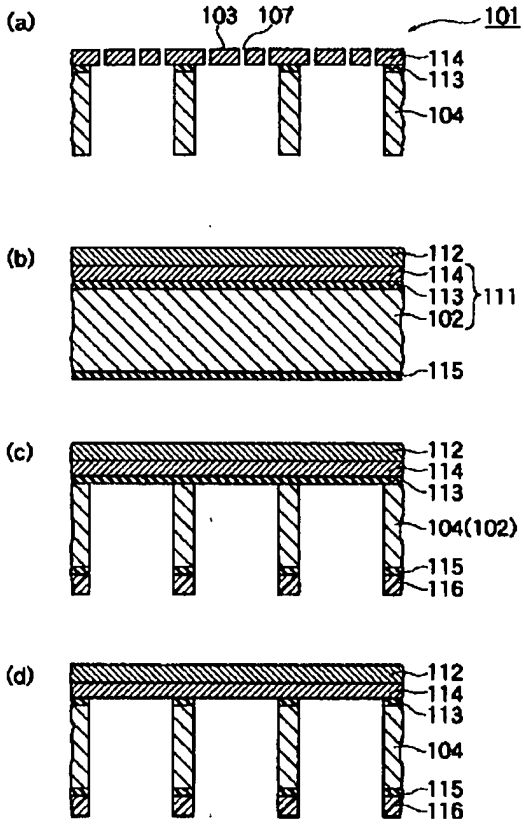
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

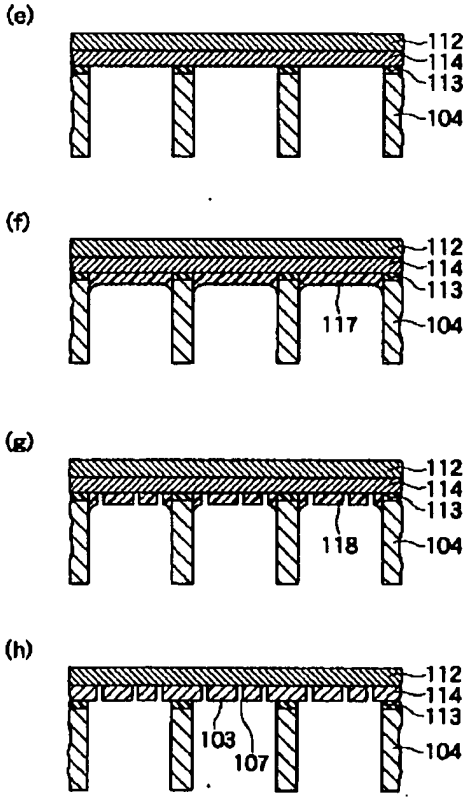
[Drawing 1]



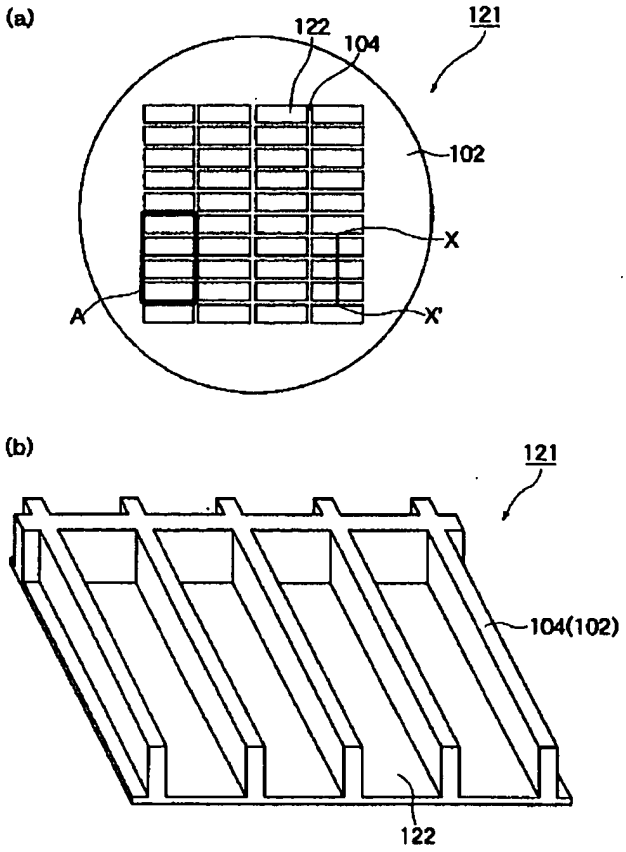
[Drawing 2]



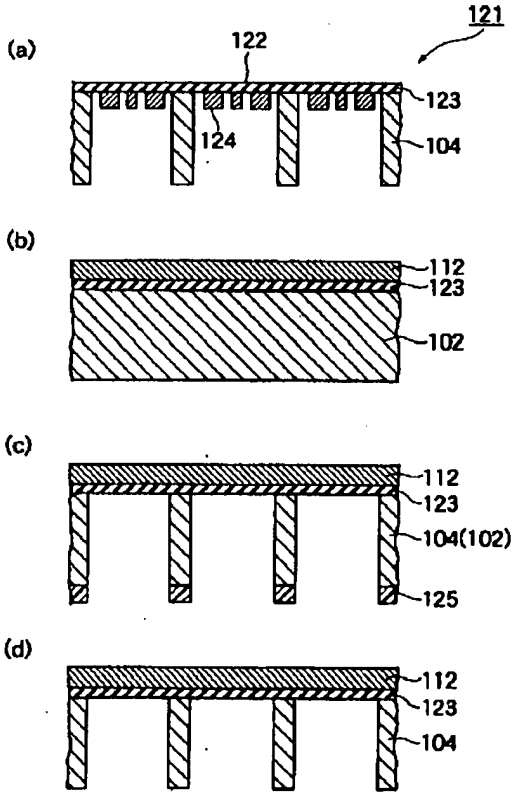
[Drawing 3]



[Drawing 4]

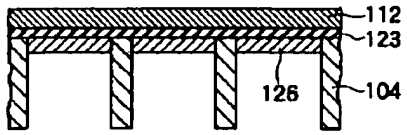


[Drawing 5]

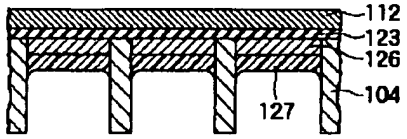


[Drawing 6]

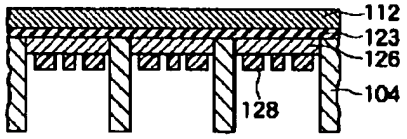
(e)



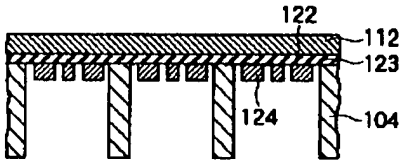
(f)



(g)

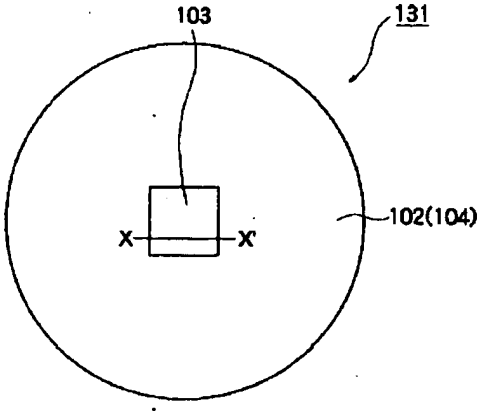


(h)

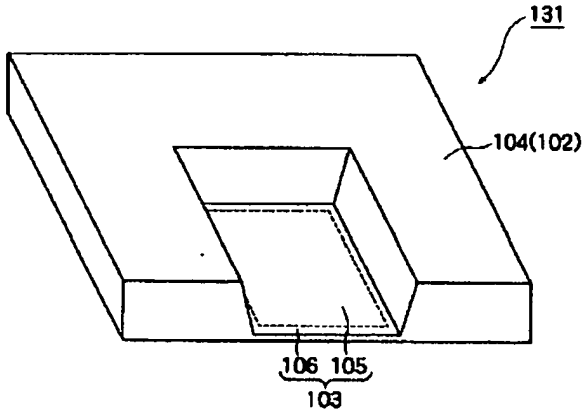


[Drawing 7]

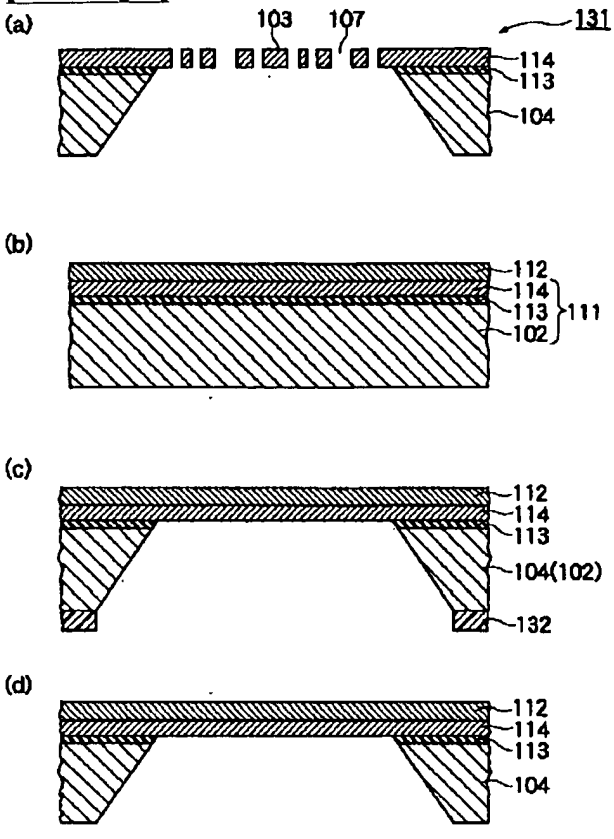
(a)



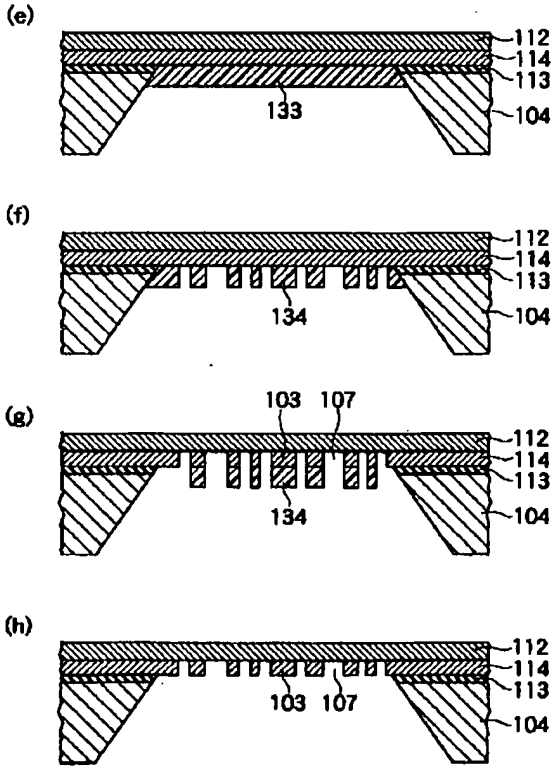
(b)



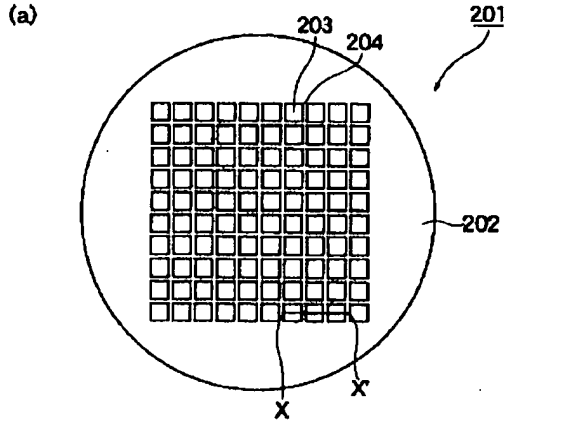
[Drawing 8]



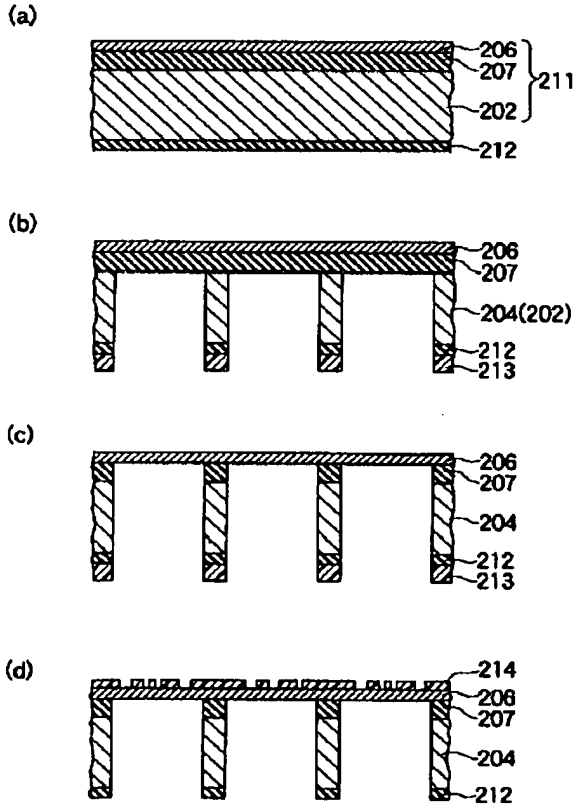
[Drawing 9]



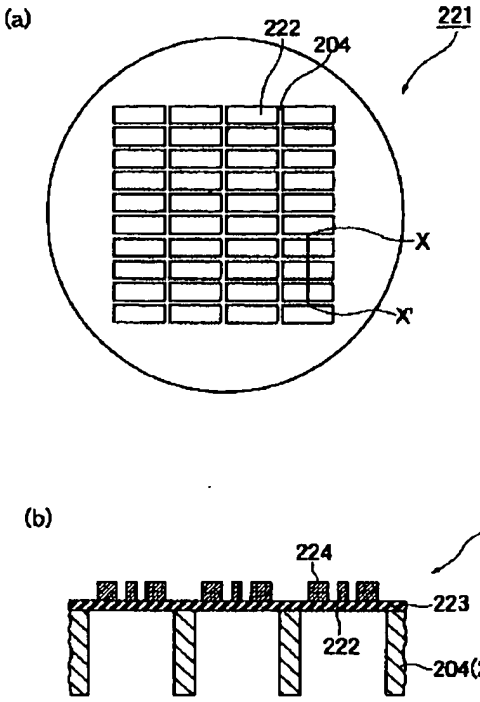
[Drawing 10]



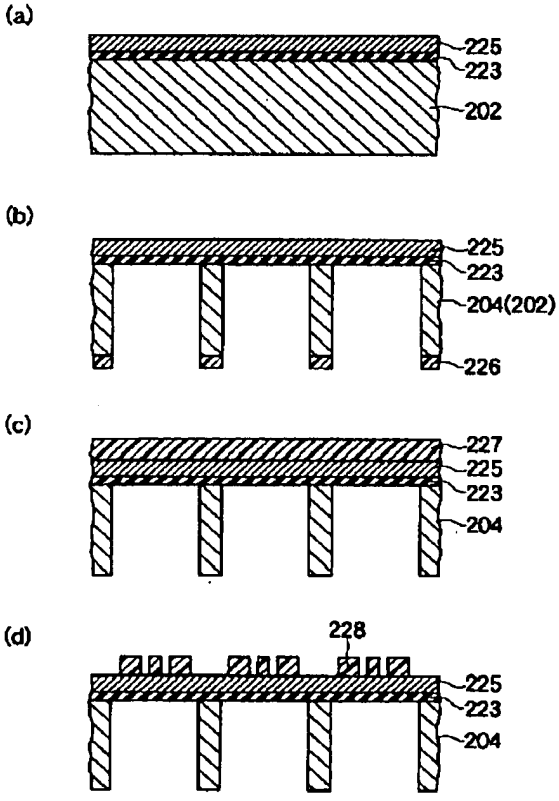
[Drawing 11]



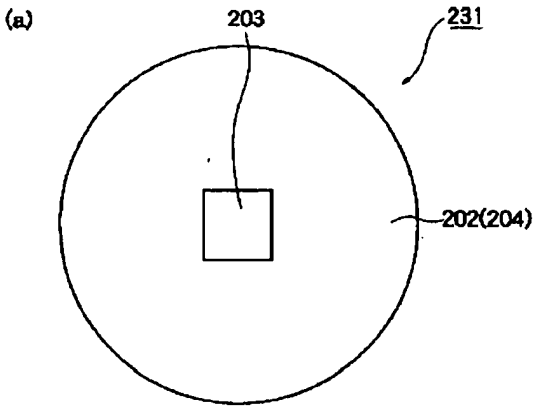
[Drawing 12]

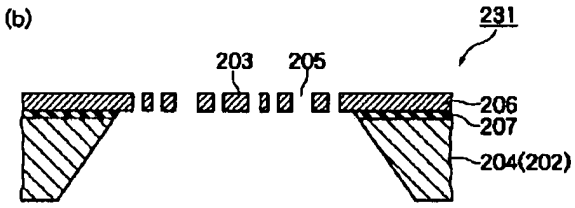


[Drawing 13]



[Drawing 14]


(a)
203
231
202(204)


(b)
231
203
205
206
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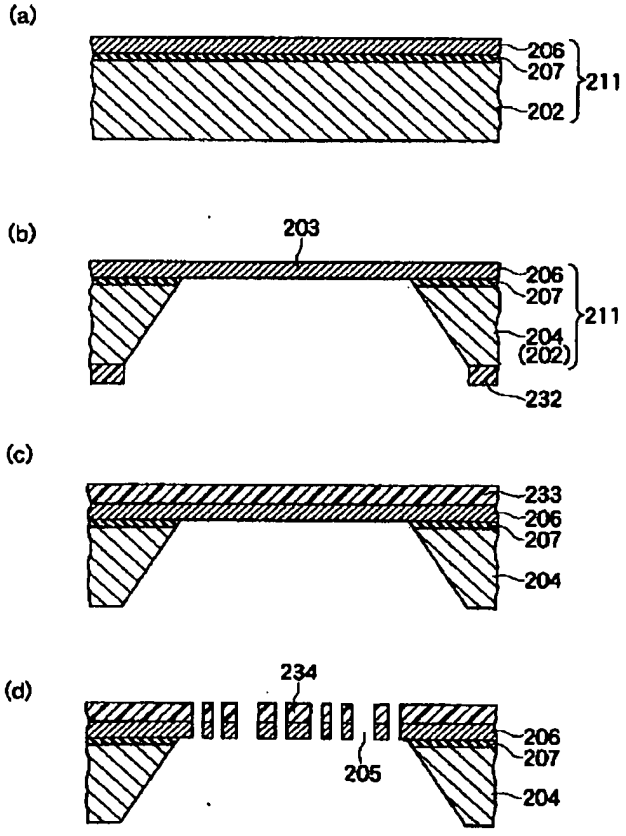
204(202)

[Drawing 15]


(a)
206
207
211
202
(b)
203
206
207
211
204
(202)
232
(c)
233
206
207
204
(d)
234
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[Translation done.]